

These pictures are computer simulations, and show the result of an analogue integrator. In the HRI decoder, a digital integrator is used. The split-phase signal is first amplified to TTL level, and instead of just one sample per bit, 64 samples are taken. If 32 or more of these samples result in "5 V", the received bit is considered to be a '1', otherwise a '0' is assumed.

Constructing the Hardware.

The decoder functions described in the previous section may all be constructed by means of digital TTL or HCMOS standard IC's. This, however, will result in many components. Note that HRPT uses 10-bit words, while standard digital IC's are organized for 4 or 8 bits. Also, the PCB design will not be that easy. Another way would be to use programmable logic like EPROM's and PLA's, but these components are limited because of their internal architecture.

A much better solution is to use a so-called FPGA (Field Programmable Gate Array), a device that is excellent in realising complex random logic. As the name says, it is programmed "in the field", which means that with one piece of hardware, several applications can be realised. It is just a matter of changing ROM's (or selecting another bank in an EPROM) to switch from one application to another. For the price of one item of hardware you get HRPT, CHRPT and HRI decoders. I have also designed generators for each format to test the software and hardware, bringing the total number of applications to six. The only extra hardware needed is a switch to select one of the applications. The largest usable EPROM is a 27C512, which can hold the code for up to 8 applications.

There are a few disadvantages. FPGA's are not commonly used by amateurs, so are a bit hard to come by. But with a bit of searching and asking, it is possible to find them.

Another problem is that dedicated (expensive) software is needed to make the design and to translate it into the code to be loaded into the EPROM.

I used Xilinx FPGA's because I was able to use the design software for these devices. The EPROM content can be downloaded from my homepage. For future designs the Atmel FPGA's are interesting because free software is available to do the design.

Principal FPGA

Fig.8 shows a rough overview of the architecture of the FPGA employed. It consists of an array of simple logical blocks (B). Each block contains two flip-flops (1-bit memories) and a programmable logical gate with 5 inputs. With this simple block it is possible to construct a 2-bit counter or a 2-bit shift register, etc.