

Between the blocks is a grid of wires (W), used to interconnect the logical blocks, to form more complex functions. The connections between wires and logical blocks are also programmable. The pins are shown around the boundaries. Each pin is programmable as input or output (tri-stateable, if needed), and can be connected to the logical blocks. The figure shows an array of 4×4 blocks and 20 pins. The FPGA used contains an array of 12×12 blocks and 84 pins. With this type nearly any kind of digital circuit is possible, with a maximum equivalent of 288 flip-flops and many hundreds of gates (AND gates, OR gates etc.).

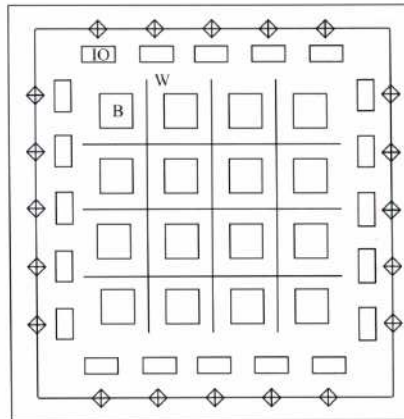


Fig.8 - Architecture of the FPGA

The program has to be stored in an EPROM. The FPGA contains some extra logic to read the content of the EPROM. As soon as power is connected, the FPGA connects an address counter to some of the pins. These pins have to be connected to the address pins of the EPROM. Data from the EPROM is loaded into the FPGA via additional pins in a fraction of a second, and in this way all the logic-block configurations, inter-block connections and input/output pin configurations are loaded. Once all data are loaded, the FPGA disconnects the EPROM and switches into functional mode. The EPROM is not needed again until power is switched off and on again.

Note that there is a big difference with a microprocessor. Instead of reading and executing one instruction at a time, the FPGA reads the complete code in one operation.

The FPGA is suitable for containing a C/HRPT or HRI-decoder. A RAM module is needed for the elastic store. The RAM needs some logic to generate addresses and to store and extract the data, for which a second FPGA is used. Because there is plenty of logic power available, just one simple dynamic RAM-module is needed. The FPGA takes care of storing 12-bit data into the 4-bit dynamic RAM, activating refresh-actions in the RAM, and interfacing between the decoder at one end and the parallel port of the PC at the other.

(There are FPGA's big enough to contain both decoder and elastic store. These types are however much more expensive, and less easy to obtain in very small quantities.)

To summarise, just 2 FPGA's, one RAM, an EPROM and a few passive components like resistors and capacitors are needed for the hardware.