

In the figure, following the second strobe pulse, the *readyn* signal stays high for a longer time - apparently the buffer is empty, so there is no new data to read. The alarm LED in the right lights if there is a buffer overflow. It should turn off after a few seconds as soon as recording starts.

Six of the data wires are also used to select channels. The parallel port is used bi-directionally, and for this, 2 more signals are added:

- \* Output enable, to switch off the data outputs of the second FPGA. The parallel port is now able to send data from PC to decoder.
- \* Write enable, a control signal to store the channel selection into the first FPGA.

**Fig.11** shows how this is done:

- \* The PC makes OEN ("Output Enable Not") high (via the "auto-feed" pin of the parallel port). This will cause the decoder to switch off its outputs.
- \* The PC switches the parallel port to "output" mode.
- \* The 6-bit channel info is sent to the parallel port data output.
- \* The PC makes WEN ("Write Enable Not") low for a while. This will cause the decoder to read in the channel info.
- \* The parallel port is switched back to input mode.
- \* The PC makes OEN low again, and the decoder outputs are switched on.

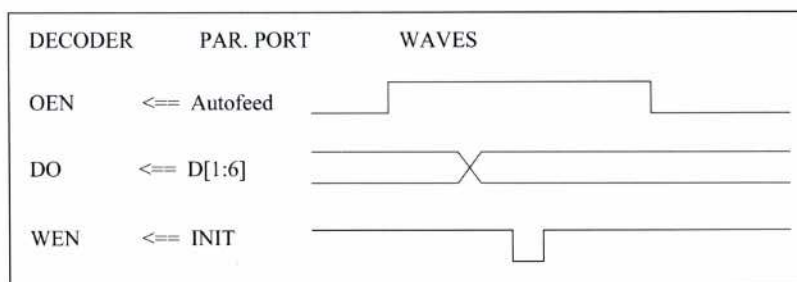


Figure 11 - Channel Selection

The elastic store needs a square wave ("clock"). This is generated by an oscillator in the FPGA. The 4.43 MHz xtal used is easy to obtain, and cheap; every PAL color TV contains one. The actual frequency is not critical; any value between 1 and 5 MHz is OK.