

The start-of-frame bit is used by the software to save lines in such a way that they are easily traced back during play-back. This bit is high during the first recorded word. The software will respond by saving the bits of the previous line to disk.

The type of RAM used is a dynamic one, organized as 256 words of 4 bits each. The FPGA is programmed in such a way that the 12 incoming bits are written and read in 3 steps into/from RAM. In this way, just one RAM module is needed. Also, the FPGA contains all refresh functionality for the dynamic RAM.

The communication with the parallel port is achieved with 14 wires:

- * 12 wires for the data (using data and 4 status bits of the parallel port)
- * A data strobe input
- * A ready signal output

Fig.10 shows some signals on the parallel port. The following actions take place:

- * The decoder sends new data to its output
- * The *readyn* ("ready not") signal goes low to signal to the PC that new data are available (*readyn* is inverted, so '0' means "ready")
- * The software reads the data from the parallel port, then makes the strobe pin low for a while
- * The decoder receives this strobe and makes *readyn* ("Not ready") high to signal the PC to wait
- * The decoder sends new data on the output and makes *readyn* low again
- * . . . and so on . . .

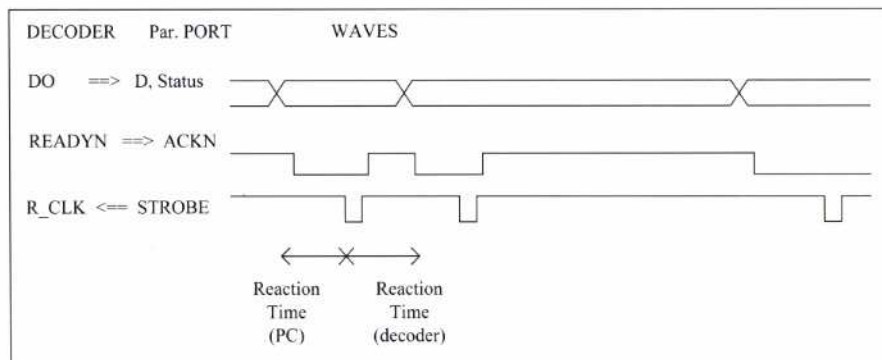


Figure 10 - Communication between Decoder and PC