

A Closer Look at the Bit-extraction

The conversion of the demodulated (split-phase) signal into a serial bit stream needs special attention. In the current decoder this is done in the following way:

The split-phase signal is converted into a TTL-level signal (done in the receiver, by means of a simple comparator). A PLL then locks on to this signal, and a counter is used to generate two samples for each bit. Every alternate sample is taken to get the actual bits.

This method works fine for strong signals like HRPT, but with HRI the received signal is too weak to produce a usable picture. **Fig. 7a** shows the original (transmitted) and received split-phase signal before it is translated into TTL level. The needles at the bottom show when a sample is taken. If the signal is positive at the sampling time the received bit is considered to be a '1', otherwise it is a '0'. The picture shows that first a '1' is transmitted, then a '0'.

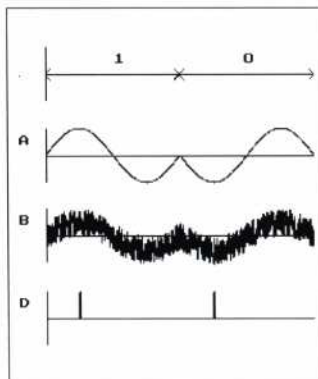


Fig.7a

Sampling digital data, with noise (left) and after noise filtering using an integrator (right)

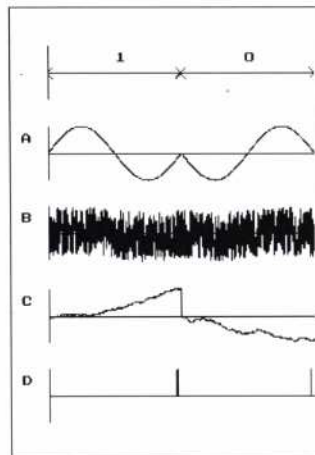


Fig.7b

In the event of noise, there is a high chance of an incorrect value being sampled. No error correction is possible with HRI (and HRPT), so these faulty bits will result in speckles in the picture or, even worse, loss of decoder synchronisation.

Sampling the signal this way means that a large part of the received signal is not used. By means of a so-called integrator, it is possible to use the whole signal when taking the decision on which value the received bit has. This is shown in **Fig. 7b**. The received signal (B) is so weak that it is very hard to see what is transmitted. Signal (C) shows the result after integration: a very big improvement!