

The FPGA contains a special inverter which can be used as an oscillator. Together with some external components a simple VCO is constructed. L1, C1, C2 and varicap D1 determine the frequency. R3, R4 and C3 act as a low pass filter. Pin 50 is the output of the phase comparator, which is a simple EXOR in the FPGA. Farther to the right a LED labelled 'err' illuminates if there are data errors and/or PLL lock problems. The dual-LED shows if the decoder is in-sync

- \* Red = out-sync
- \* Green = in-sync
- \* Yellow = going in-sync or going out-sync (this takes just 1/6 second)

### Elastic Store

The right-hand FPGA (IC4) acts together with the RAM (IC5) as the data buffer (elastic store). It loads the 10-bit data from the decoder FPGA into the RAM. At the same time, data are read from this RAM and sent to the PC's parallel port. The FPGA manages these two data streams. For example, if the PC is too fast, data transfer has to stop for a while until there is new data available in the RAM. This is what normally happens

Data are saved from the decoder into RAM. If the recording software is inactive, old data will be overwritten. (The RAM can hold a few seconds of HRPT data, depending how many channels are selected). As soon as the software starts recording, bits are transferred from RAM to PC. This will happen at full speed until there are no data left. Now, the PC will read data at the same rate as data are applied by the decoder. Once a line of data has been read, the software will save data (11090 words) to the hard disc. No data are read to the PC so the elastic store fills up with data. As soon as the PC has completed saving the previous line, it starts again, reading new data from the buffer. (See also **Fig. 6**)

The buffer is able to handle 64k words of 12 bits each. These are:

- \* 10 data bits
- \* in-sync bit
- \* start-of-frame bit

The in-sync bit is used by the software to start recording as soon as a usable signal is received. This bit is also saved once for each recorded line, in this way making it possible to detect bad lines afterwards. These lines give very disturbed pictures, but the software can replace a bad line by an adjacent line which was received correctly. Normally, the in-sync bit is always high during record.