

### The Schematic

**Fig.9** (overleaf) shows the schematic of the complete decoder/generator. The two big square boxes (IC1, IC4) are the FPGA's. The left half of the schematic is the actual decoder/generator, while the right one acts as controller for the elastic store.

The EPROM (IC2) contains the programs to load into the 2 FPGA's. A 512k type can contain 8 programs, which is enough for decoders and generators for HRPT, CHRPT and HRI. Note that just one of these programs is active at a time. To use a decoder and generator at the same time, two systems are needed. (It is possible to construct a very simple HRPT generator, just good enough to test the input part of the decoder. This is much cheaper than making 2 complete systems.)

### Loading the EPROM Data

The EPROM is connected to the left FPGA with 13 address pins. After power-up, the FPGA starts a counter connected to these pins, and the content of the EPROM is read via the 8 data pins. There are 3 address pins left on the EPROM, used to select 1 of 8 segments in the EPROM. These segments contain the HRPT, CHRPT and HRI decoders and generators (there is space for 1 more decoder/generator pair). The first half of the loaded code programs the left FPGA as decoder or generator; the second part contains the program for the elastic store controller. The left FPGA converts this data into a serial stream, which is transferred to the second FPGA via pins 74 and 73. In this way just 1 EPROM is needed to program both FPGA's.

As soon as the program is loaded into the FPGA, the EPROM is disabled. Most pins connected to the EPROM are now available for functional mode, and in this case they are used to output the 10 data bits. Pin 55 is a special pin, which, if pulled low, causes the FPGA to reload itself. The components connected to this pin take care of automatic reloading of the FPGA as soon as another segment of the EPROM is chosen. This means that disconnecting the power is not needed. (Unfortunately, this doesn't work if the highest address is changed by means of switch SX. In this case a short disconnection of power is needed to reload the FPGA.)

### Decoder/Generator Diagram [Fig.9]

At the bottom-left of are shown the decoder's data input and the generator's data output. The parallel port is located at upper right. The connections from parallel port to the left-hand FPGA (via the diodes) are there for channel selection. In HRI mode these connections are not used because the HRI decoder doesn't contain a channel selector. Beneath IC1 there are six LED's showing which channels are selected.